U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
M122-2378SERIAL NO.
10/630,427withLIST OF ART CITED BY APPLICANT
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Wendell P. NobleFILING DATE
July 29, 2003GROUP
Unassigned 2813

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
AL	AA	5,830,797	11/98	Cleaves			
	AB						
	AC						
	AD						
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	AK						
	AL						
	AM						
	AN						
	AO						
	AP						

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	AQ						
	AR						
	AS						

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)


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		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2378		SERIAL NO. 10/630,427with	
		LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Wendell P. Noble	
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GROUP Unassigned 2813							
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<i>AS</i>	AA	5,604,159	02/97	Conper, et al.			
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	AC	6,136,701	10/00	Shin			
	AD	6,291,286	09/01	Hsiao			
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	AK						
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	AN						
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FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
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EXAMINER <i>Wendell P. Noble</i>				DATE CONSIDERED <i>6/11/04</i>			
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				FILING DATE Filed Herewith	GROUP Unassigned 2813

U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AL	AA	5,539,229	07/96	Noble, Jr., et al.			
AL	AB	5,214,603	05/93	Dhong, et al.			
AL	AC	4,604,162	08/86	Sobczak			
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AL	AF	5,599,724	02/97	Yoshida			
AL	AG	5,846,854	12/98	Giraud, et al.			
AL	AH	5,011,783	04/91	Ogawa, et al.			
AL	AI	4,700,461	10/87	Choi, et al.			
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Document Number	Date	Country	Class	Subclass	Translation		
					Yes	No	
AQ 0 720 221 A1	07/96	EPO					
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AT		Davari et al., "A Variable-Size Shallow Trench Isolation (STI) Technology With Diffused Sidewall Doping For Submicron CMOS,"
		IEDM Technical Digest, International Electron Devices Meeting, San Francisco, CA, Dec. 11-14, 1988, pp. 92-95.
AU		Bakeman et al., "A High Performance 16-Mb Dram Technology," 1990 Symposium on VLSI Technology Digest of Technical Papers,
		1990 VLSI Technology Symposium, Honolulu, HI, June 4-7, 1990, pp. 11-12.

EXAMINER <i>Wendell P. Noble</i>	DATE CONSIDERED 6/11/04
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EV317134177

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					FILING DATE Filed Herewith	GROUP Unassigned 2813
U.S. PATENT DOCUMENTS						
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
 	AA	5,241,211	08/93	Toshiro		
	AB					
	AC					
FOREIGN PATENT DOCUMENTS						
	Document Number	Date	Country	Class	Subclass	Translation Yes No
	AP					
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)						
 	AS	Suma et al., "An SOI-DRAM With Wide Operating Voltage Range by CMOS/SIMOX Technology," <i>IEEE Journal of Solid-State Circuits</i> , November 1994, pp. 1323-1329.				
		Kuge et al., "SOI-DRAM Circuit Technologies For Low Power High Speed Multigiga Scale Memories", <i>IEEE Journal of Solid-State Circuits</i> , April 1996, pp. 586-591.				
 		Y. Kohyama et al., "Buried Bit Line Cell for 64MB DRAMs," <i>IEEE, 1990 Symposium on VLSI Technology</i> , pp. 17, 18.				
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 		Takahiro Onal et al., "SEPIA: A New Isolation Structure for Soft-Error-Immune LSI's," 1993 <i>IEEE</i> , 3 pages.				
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<small>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small>						